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Question Paper Code : 21464

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Eighth/Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 — VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008/2010)

(Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Determine the drain current of short channel NMOS transistor for the following measurements V_{DS} = 1.5 V, V_{GS} = 2 V, V_{BS} = 0 V, V_{TO} = 0.43 V. Assume V_{DSAT} = 0.6V, K_n' = 110 uA/V^2, λ = 0.1 V^{-1}, γ = 0.4 and W/L = 0.4/0.25.

2. Define any two Layout design rules.

3. List out the limitations of the constant voltage scaling.

4. Draw the small signal model of a MOSFET.

5. Differentiate between latch and flipflop.

6. List out the techniques used for low power logic design.

7. What is need for testing VLSI circuits?

8. Define boundary scan test.

9. Distinguish between blocking and non-blocking assignments in Verilog HDL.

10. Write Verilog HDL code for a full adder using structural modeling.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the DC transfer characteristics of CMOS inverter. (16)

Or

(b) (i) Explain in detail of C-V Characteristics of MOSFET. (8)

(ii) Explain any one process enhancement method and one manufacturing issue in detail. (8)

12. (a) (i) Explain the power dissipation of static CMOS design in detail. (8)

(ii) Define Logical Effort and reason-out why mostly NAND gates are used to realize the combinational circuits rather than NOR gates. (4)

(iii) Discuss resistance and capacitance of a interconnect. (4)

Or

(b) (i) Explain the constant field scaling. Write its advantages. (8)

(ii) List out all device characterization and explain any two. (8)

13. (a) (i) Consider the circuit of Figure. 13(a) (i). (8)

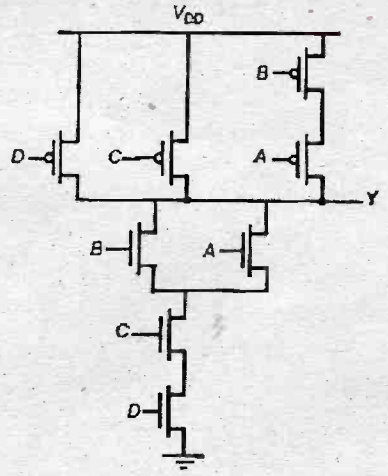

Figure. 13(a) (i)

(1) What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

(2) What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

(3) Determine the dynamic power dissipation in the logic gate. Assume V_{DD} = 2.5V, *Cout* = 30 *fF* and *fclk* = 250 MHz.

(ii) Show that the output logic level of pseudo NMOS logic is dependent on the size of the transistor. (4)

(iii) List out the issues present in Dynamic CMOS logic design. Explain any two. (4)

Or

(b) (i) Consider the circuit shown in Fig. 13(b) (i).

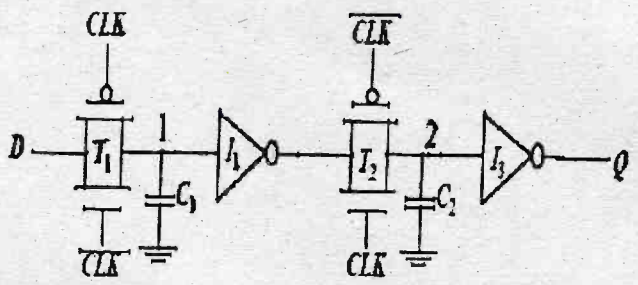

Fig. 13(b) (i)

(1) State whether the circuit is a latch or edge triggered register. Justify your answer.

(2) In the circuit consider C1 and C2 as the intrinsic capacitances of inverters and transmission gates. Assuming ideal clock, compute the setup time, hold time and propagation delay in terms of the inverter I1, I2 delay and transmission gate T1, T2 delay. (8)

(ii) Explain the true single phase clock latch. (8)

14. (a) Briefly discuss the following terms : (16)

(i) Testers

(ii) Test fixtures

(iii) Test programs.

Or

(b) (i) Explain the Silicon debug principles in detail (8)

(ii) Explain the Manufacturing test principles in detail (8)

15. (a) Write Verilog HDL code for an 8:3 priority encoder using

(i) casex statement

(ii) data flow modeling. (16)

Or

(b) (i) Write Verilog HDL code for an 8-bit ripple carry adder (10)

(ii) Briefly describe the difference between inertial delay and Transport delay. (6)
